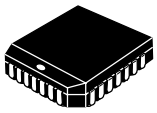
MC10H643, MC10H643

Dual Supply ECL to TTL 1:8 Clock Driver

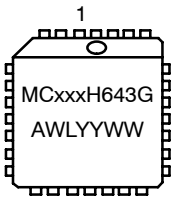
ON Semiconductor®

http://onsemi.com



PLCC−28
FN SUFFIX
CASE 776

MARKING DIAGRAM*



xxx	= 10 or 100
A	= Assembly Location
WL	= Wafer Lot
YY	= Year
WW	= Work Week
G	= Pb−Free Package

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

Description

The MC10H/100H643 is a dual supply, low skew translating 1:8 clock driver. Devices in the ON Semiconductor H643 translator series utilize the PLCC−28 for optimal power pinning, signal flow through and electrical performance. The dual−supply H643 is similar to the H641, which is a single−supply 1:9 version of the same function.

The device features a 48 mA TTL output stage, with AC performance specified into a 50 pF load capacitance. A Latch is provided on−chip. When LEN is LOW (or left open, in which case it is pulled LOW by the internal pulldowns) the latch is transparent. A HIGH on the enable pin ($\overline{EN}$) forces all outputs LOW.

The 10H version is compatible with MECL 10H™ ECL logic levels. The 100H version is compatible with 100K levels.

Features

- ECL/TTL Version of Popular ECLinPS™ E111
- Low Skew Within Device 0.5 ns
- Guaranteed Skew Spec Part−to−Part 1.0 ns
- Latch
- Differential Internal Design
- V_{BB} Output
- Dual Supply
- Reset/Enable
- Multiple TTL and ECL Power/Ground Pins
- Pb−Free Packages are Available*

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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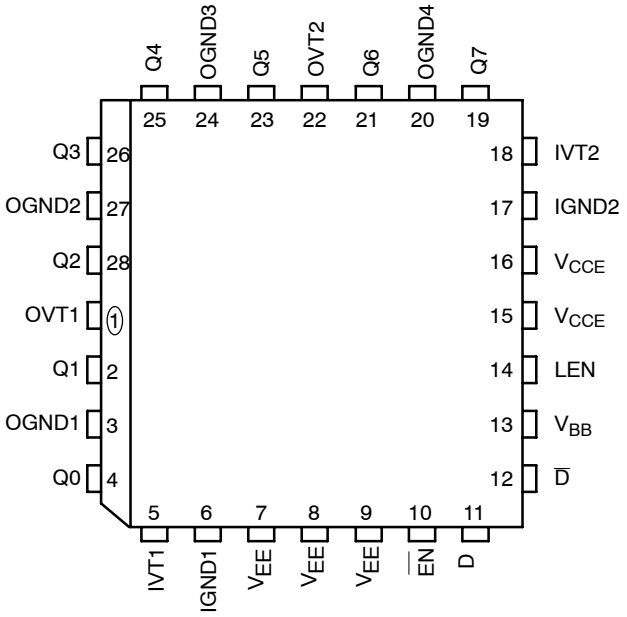


Figure 1. Pinout: PLCC−28
(Top View)

Table 1. PIN DESCRIPTION

PIN	FUNCTION
OGND	TTL Output Ground (0V)
OVT	TTL Output V_{CC} (+5.0V)
IGND	Internal TTL GND (0V)
IVT	Internal TTL V_{CC} (+5.0V)
V_{EE}	ECL V_{EE} (−5.2/−4.5V)
V_{CCE}	ECL Ground (0V)
D, $\overline{D}$	Signal Input (ECL)
V_{BB}	V_{BB} Reference Output
Q0 − Q7	Signal Outputs (TTL)
$\overline{EN}$	Enable Input (ECL)
LEN	Latch Enable Input (ECL)

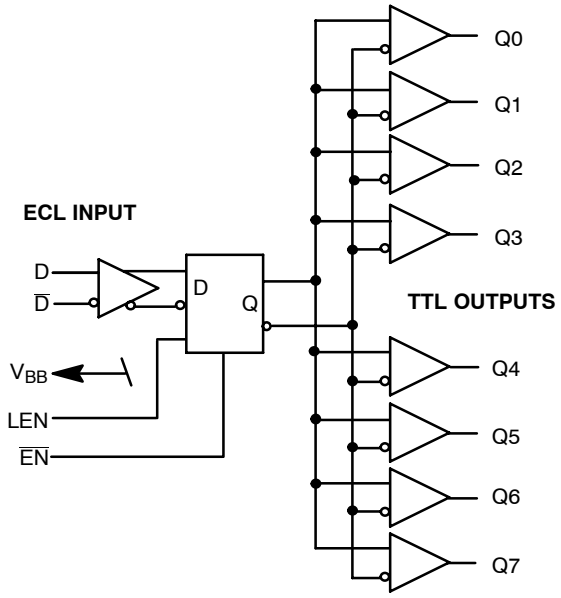


Figure 2. Logic Diagram

Table 2. TRUTH TABLE

D	LEN	EN	Q
L	L	L	L
H	L	L	H
X	H	L	Q_O
X	X	H	L

Table 3. DC CHARACTERISTICS (IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version))

Symbol	Characteristic		Condition	0°C		25°C		85°C		Unit
				Min	Max	Min	Max	Min	Max	
I_{EE}	Power Supply Current	ECL	V_{EE} Pins	–	42	–	42	–	42	mA
I_{CCL}		TTL	Total all OVT and IVT pins	–	106	–	106	–	106	mA
I_{CCH}				–	95	–	95	–	95	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 4. 10H ECL DC CHARACTERISTICS (IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version))

Symbol	Characteristic	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	– 0.5	255 –	– 0.5	175 –	– 0.5	175 –	μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1170 −1950	−840 −1480	−1130 −1950	−810 −1480	−1070 −1950	−735 −1450	mV
V_{BB}	Output Reference Voltage	−1380	−1270	−1350	−1250	−1310	−1190	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 5. 100H ECL DC CHARACTERISTICS (IVT = OVT = 5.0 V ±5%; V_{EE} = −4.2 V to −5.5 V (100H))

Symbol	Characteristic	0°C		25°C		85°C		Unit
		Min	Max	Min	Max	Min	Max	
I_{INH} I_{INL}	Input HIGH Current Input LOW Current	– 0.5	255 –	– 0.5	175 –	– 0.5	175 –	μA
V_{IH} V_{IL}	Input HIGH Voltage Input LOW Voltage	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	−1165 −1810	−880 −1475	mV
V_{BB}	Output Reference Voltage	−1380	−1260	−1380	−1260	−1380	−1260	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 6. DC TTL CHARACTERISTICS (IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±5% (10H Version); V_{EE} = −4.2 V to −5.5 V (100H Version))

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
V_{OH}	Output HIGH Voltage	I_{OH} = −3.0 mA I_{OH} = −15 mA	2.5 2.0	– –	2.5 2.0	– –	2.5 2.0	– –	V
V_{OL}	Output LOW Voltage	I_{OH} = 48 mA	–	0.5	–	0.5	–	0.5	V
IOS	Output Short Circuit Current	V_{OUT} = 0 V	−100	−225	−100	−225	−100	−225	mA

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

Table 7. AC CHARACTERISTICS (IVT = OVT = 5.0 V ±5%; V_{EE} = −5.2 V ±10% (10H); −4.2 V to −5.5 V (100H); V_{CCE} = GND)

Symbol	Characteristic	Condition	0°C		25°C		85°C		Unit
			Min	Max	Min	Max	Min	Max	
t_{PLH}	Propagation Delay to Output D LEN $\overline{EN}$	CL = 50 pF	 4.0 3.5 3.5	 5.0 5.5 5.5	 4.1 3.5 3.5	 5.1 5.5 5.5	 4.4 3.9 3.9	 5.4 5.9 5.9	ns
t_{SKEW}	Within−Device Skew	(Note 1)	–	0.5	–	0.5		0.5	ns
tw	Pulse Width Out HIGH or LOW @ f_{out} = 50MHz	CL = 50 pF (Note 2)	9.0	11.0	9.0	11.0	9.0	11.0	ns
t_s	Setup Time D		0.75	–	0.75	–	0.75	–	ns
t_h	Hold Time D		0.75	–	0.75	–	0.75	–	ns
t_{RR}	Recovery Time LEN $\overline{EN}$		 1.25 1.25	 – –	 1.25 1.25	 – –	 1.25 1.25	 – –	ns
t_{pw}	Minimum Pulse Width LEN $\overline{EN}$		 1.5 1.5	 – –	 1.5 1.5	 – –	 1.5 1.5	 – –	ns
t_r t_f	Rise / Fall Times 0.8 V – 2.0 V	CL = 50 pF	–	1.2	–	1.2	–	1.2	ns

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

1. Within−Device skew defined as identical transitions on similar paths through a device.
2. Pulse width is defined relative to 1.5 V measurement points on the output waveform.

ORDERING INFORMATION

Device	Package	Shipping†
MC10H643FN	PLCC−28	37 Units / Rail
MC10H643FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC10H643FNR2	PLCC−28	500 / Tape & Reel
MC10H643FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel
MC100H643FN	PLCC−28	37 Units / Rail
MC100H643FNG	PLCC−28 (Pb−Free)	37 Units / Rail
MC100H643FNR2	PLCC−28	500 / Tape & Reel
MC100H643FNR2G	PLCC−28 (Pb−Free)	500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

Resource Reference of Application Notes

AN1405/D – ECL Clock Distribution Techniques

AN1406/D – Designing with PECL (ECL at +5.0 V)

AN1503/D – ECLinPS™ I/O SPiCE Modeling Kit

AN1504/D – Metastability and the ECLinPS Family

AN1568/D – Interfacing Between LVDS and ECL

AN1672/D – The ECL Translator Guide

AND8001/D – Odd Number Counters Design

AND8002/D – Marking and Date Codes

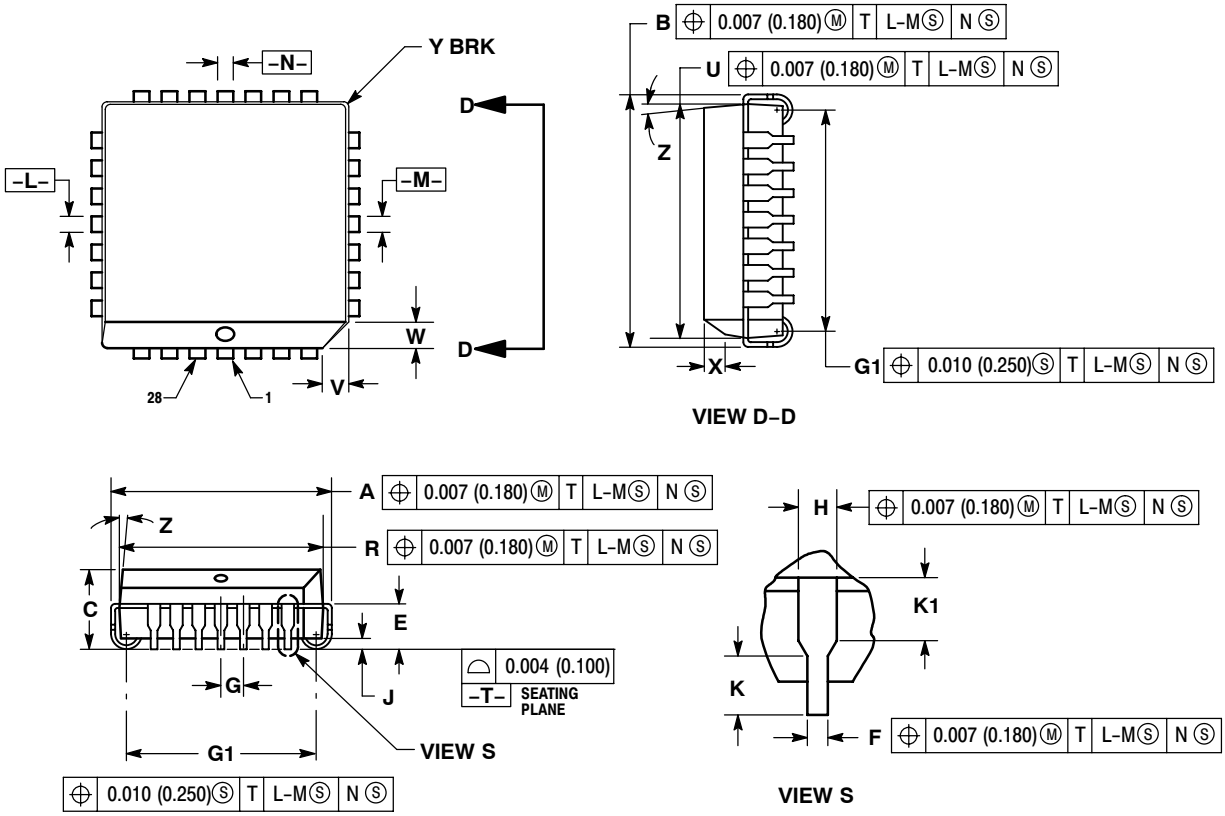
AND8020/D – Termination of ECL Logic Devices

AND8066/D – Interfacing with ECLinPS

AND8090/D – AC Characteristics of ECL Devices

PACKAGE DIMENSIONS

PLCC−28
FN SUFFIX
PLASTIC PLCC PACKAGE
CASE 776−02
ISSUE E



NOTES:
1. DATUMS −L−, −M−, AND −N− DETERMINED WHERE TOP OF LEAD SHOULDER EXITS PLASTIC BODY AT MOLD PARTING LINE.
2. DIMENSION G1, TRUE POSITION TO BE MEASURED AT DATUM −T−, SEATING PLANE.
3. DIMENSIONS R AND U DO NOT INCLUDE MOLD FLASH. ALLOWABLE MOLD FLASH IS 0.010 (0.250) PER SIDE.
4. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
5. CONTROLLING DIMENSION: INCH.
6. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM BY UP TO 0.012 (0.300). DIMENSIONS R AND U ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, TIE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
7. DIMENSION H DOES NOT INCLUDE DAMBAR PROTRUSION OR INTRUSION. THE DAMBAR PROTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE GREATER THAN 0.037 (0.940). THE DAMBAR INTRUSION(S) SHALL NOT CAUSE THE H DIMENSION TO BE SMALLER THAN 0.025 (0.635).

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.485	0.495	12.32	12.57
B	0.485	0.495	12.32	12.57
C	0.165	0.180	4.20	4.57
E	0.090	0.110	2.29	2.79
F	0.013	0.019	0.33	0.48
G	0.050 BSC		1.27 BSC	
H	0.026	0.032	0.66	0.81
J	0.020	---	0.51	---
K	0.025	---	0.64	---
R	0.450	0.456	11.43	11.58
U	0.450	0.456	11.43	11.58
V	0.042	0.048	1.07	1.21
W	0.042	0.048	1.07	1.21
X	0.042	0.056	1.07	1.42
Y	---	0.020	---	0.50
Z	2°	10°	2°	10°
G1	0.410	0.430	10.42	10.92
K1	0.040	---	1.02	---

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